

# C.U.SHAH UNIVERSITY

## Summer Examination-2017

Subject Name: CMOS VLSI Design

Subject Code: 5TE01CVD1

Branch: M.Tech (VESD)

Semester: 1

Date: 20/03/2017

Time: 10:30 To 01:30

Marks: 70

### Instructions:

- (1) Use of Programmable calculator and any other electronic instrument is prohibited.
  - (2) Instructions written on main answer book are strictly to be obeyed.
  - (3) Draw neat diagrams and figures (if necessary) at right places.
  - (4) Assume suitable data if needed.
- 

### SECTION – I

- Q-1** Define the following terms **(07)**
- a.  $NM_H$
  - b. Transistor sizing.
  - c. Threshold Voltage.
  - d. Rise time.
  - e.  $NM_L$
  - f. Dynamic Power Consumption.
  - g. Power Delay Product.

- Q-2** Attempt all questions **(14)**
- (a) Explain the minimization of RC effect in CMOS inverter chain.
  - (b) Explain the Series and Parallel CMOS switch combinations.

**OR**

- Q-2** Attempt all questions **(14)**
- (a) Sketch a transistor-level schematic for a compound CMOS logic gate for  $Y = ((AB+C) D)'$ .
  - (b) Design and explain 3-input CMOS Ex-OR. How many transistors are required?

- Q-3** Attempt all questions **(14)**
- (a) Compare CMOS and NMOS.
  - (b) Explain Body effect. Explain how Body effect affects the threshold voltage.

**OR**

- Q-3** Attempt all questions **(14)**
- (a) Explain the Transmission gate and the tri-state inverter
  - (b) Explain the fringing effects in MOS device.



