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	Enrolln	nent No:							
			C.U.SHAH	UNIVERSIT	Y				
	Summer Examination-2017								
	Subject Name: CMOS VLSI Design								
	Subject Code: 5TE01CVD1			Branch: M.Tech (VESD)					
	Semest	er: 1	Date: 20/03/2017	Time: 10:30 To 01:30	Marks: 70				
	Instruc								
	(1) Use of Programmable calculator and any other electronic instrument is prohibited.								
	(2) Instructions written on main answer book are strictly to be obeyed.(3) Draw neat diagrams and figures (if necessary) at right places.								
	(4) Assume suitable data if needed.								
	SECTION – I								
Q-1	Define the following terms					(07)			
		NM _H Transist	tor sizing						
	c.		old Voltage.						
	d.		•						
	e.	NM_{L}							
	f.	Dynami	c Power Consumption.						
	g.	Power I	Delay Product.						
Q-2		Attemp	t all questions			(14)			
	(a)	_	_	fect in CMOS inverter chain		, ,			
	(b)	Explain	the Series and Parallel CM	IOS switch combinations.					
OR									
Q-2		_	t all questions			(14)			
	(a)		a transistor-level schema B+C) D)'.	atic for a compound CMC	OS logic gate for				
	(b)			Ex-OR. How many transisto	ors are required?				
Q-3		Attemp	t all questions			(14)			

Q-2

Q-3

- (a)
- Compare CMOS and NMOS.
 Explain Body effect. Explain how Body effect affects the threshold voltage. **(b)**

OR

Q-3 **Attempt all questions**

(14)

- Explain the Transmission gate and the tri-state inverter Explain the fringing effects in MOS device. (a)
- **(b)**



SECTION – II

Q-4		Define the following terms	(07)
	a.	Tri-state logic	
	b.	Bi-directional Pads	
	c.	Serial Multiplier	
	d.	Routing capacitance of MOS	
	e.	Pass transistor	
	f.	Latch	
	g.	Charge sharing	
Q-5		Attempt all questions	(14)
	(a)	Derive the capacitances of three regions of operation of MOS device.	` ,
	(b)	Write note on CMOS Domino logic	
		OR	
Q-5		Attempt all questions	(14)
	(a)	Draw and explain Cascade Voltage Switch logic (CVSL)	` '
	(b)	Explain Pseudo 4-phase memory structures.	
Q-6		Attempt all questions	(14)
•	(a)	Explain in detail Boundary-scan testing.	()
	(b)	Explain the design of Ripple Carry Binary Asynchronous Counter.	
		OR	
Q-6		Attempt all Questions	(14)
Q-0	(a)	Explain the design of Wallace tree multiplier circuit.	(17)
	(a) (b)	Explain the basic Dynamic MOS RAM Cell.	
	(0)	Explain the basic Dynamic Wob Kriw Cen.	

